Complete Bluetooth® solution

STLC2500D: Bluetooth V2.0/V2.1(Lisbon) + enhanced data rate on a single chip

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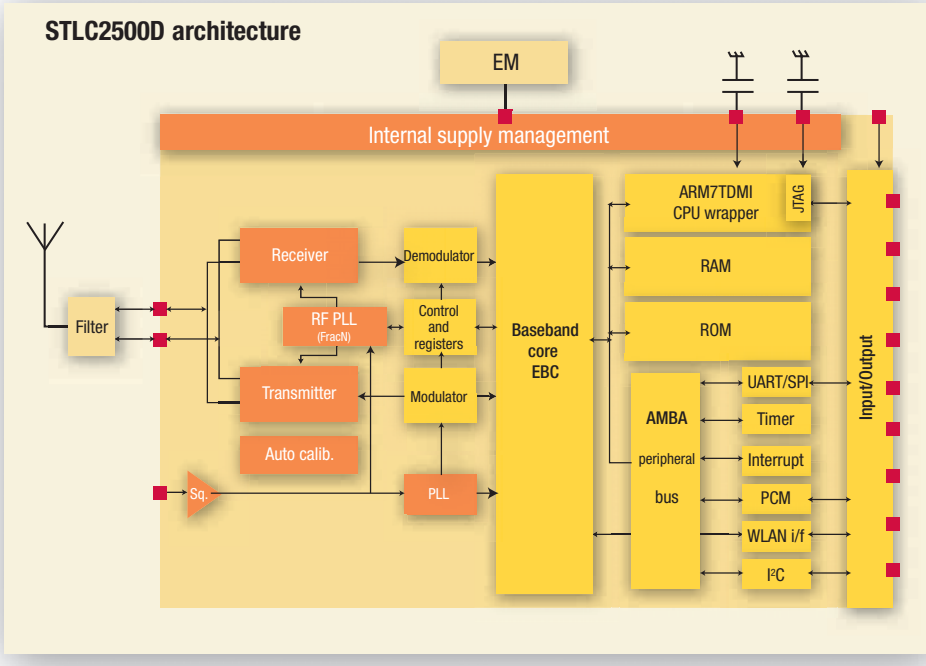
STLC2500D - Bluetooth V2.1/V2.0 + EDR (Lisbon) single chip

STMicroelectronics' STLC2500D features complete Bluetooth V2.1 + EDR Lisbon functionality with best-in-class power consumption and radio performances, making it ideal for mobile applications offering 1, 2 and 3 Mbit/s full-throughput data rates. The STLC2500D is a complete single-chip solution combining radio, baseband, processor and memory. The device can be easily integrated by manufacturers, and enables a rapid time to market, as it requires very few external components, and is supported by complete reference designs, development tools, and manufacturing guidelines. Additionally, ST has a network of regional offices that can offer customers local Bluetooth expertise.



Keys benefits

- Market's lowest power consumption in all operating modes, made possible through:
  - Leading-edge power management design
  - ST's unique HCMOS9 low-power and ultra low-leakage 0.13 µm technology
- Fully-compliant with Bluetooth specs (V2.1 + EDR)
- Full Lisbon support
- Enhanced Rx performance
- Improved Tx performance
- Full EDR throughput
- Flexible SPI interface up to 13 MHz
- Best-in-class radio performance for both basic rate and EDR
- Enhanced audio quality (such as PPEC, eSCO)
- Wireless LAN coexistence:
  - Hardware implementation with software-configurable engine to meet stringent timing requirements and enhanced priority handling, for every coexistence scheme on the market
- Small PCB footprint 6.5 mm² (including external components) (4.5 mm² package)
- Highly flexible patch RAM and ROM-upgrade technology

Leading performance

Current consumption

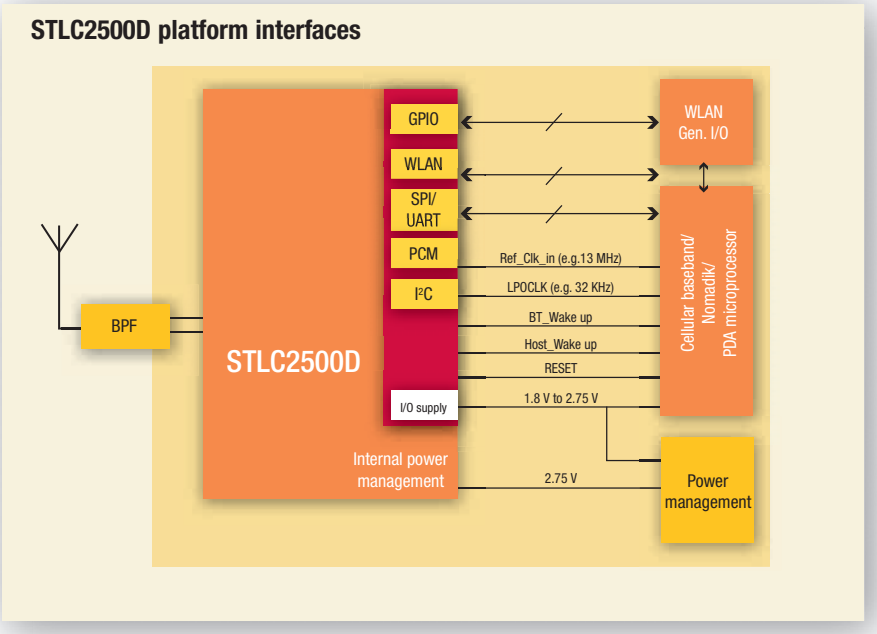
- Audio communication
  HV3: 10.25 mA, 3-EV3: 5.79 mA
- Data communication at maximal throughput
  DH1: 18.6 mA 3-DH5: 29.8 mA
- Complete power down
  1 µA

At host interface throughput 2.75 Mbit/s

Applications

The STLC2500D is designed to be easily and efficiently integrated into mobile terminal platforms. With its highly flexible hardware and software interfaces, the STLC2500D can work with virtually any silicon chip platform, including ST's award winning Nomadik® application processor.

STLC2500D platform interfaces



Flexibility is key in STLC2500D

- HCI interface
- High-speed UART and SPI/H4
- Flexible clock request functions
  - Best power saving and reduced cost of implementation
  - Flexible I/O implementation
  - Support for WLAN, Class1 extension, I²C

Chip parameter configuration has never been so easy. The STLC2500D requires only a single HCI command for configuration and parameter download.

STLC2500D

Bluetooth single-chip which makes no compromise in:

- Power consumption
- Cost
- Performance
- Size
- Technology

Features

- Supports specifications V2.1 and EDR
  - EDR feature support + all Bluetooth V1.2 errata
  - All new data rates and packet types
  - New RF carrier modulation methods for Tx
- Backward compatibility with legacy devices through extended V2.0 feature support
  - Adaptive frequency hopping (AFH)
  - Faster connections through interlaced scan for page and inquiry, RSSI
  - Extended SCO (eSCO) links
- Full Lisbon support
  - Encryption pause/resume (EPR)
  - Extended inquiry response (EIR)
  - Sniff subrating (SSR)
  - Quality of service (QoS):
    - Erroneous data delivery
    - Packet boundary flag (PBF)
  - Secure simple pairing
  - Link supervision time out (LSTO)
- Tx output power up to 8 dBm
- Point-to-point, point-to-multipoint (up to seven slaves) and scatternet capability
- Asynchronous connectionless (ACL) link supports data rates up to 2 and 3 Mbit/s
- Synchronous connection oriented (SCO) link: two simultaneous SCO channels support at 64 Mbit/s
- Pitch-period error concealment (PPEC)
  - Improved speech quality in the vicinity of interference
  - Improved integration with WLAN
- Clock support for all cellular standards
  - System clock input
  - LPO clock input
- ARM7TDMI CPU – 32-bit core
- Patch RAM to boost time-to-volume performance
- Communication interfaces
  - Fast UART (up to 4 Mbit/s) for HCI transport
  - SPI interface (up to 13 Mbit/s) for HCI transport
  - PCM interface for voice
  - Wireless LAN coexistence 2, 3, 4 wires
  - 19 programmable GPIOs
  - Fast master I^2C interface
- Ciphering support up to 128-bit keys, offering superior security over wireless technologies
- Software support
  - Low-level (up to HCI) stack
  - HCI transport layer H4
  - HCI proprietary commands (such as peripherals control)
  - Single HCI command for patch/upgrade download
- Internal power management
- Supports 1.65 to 2.85 V IO systems
  - Total number of external components limited to seven (six decoupling capacitors and one single antenna interface component)
- Auto calibration (VCO, filters)
  - No need for calibration of RF in production
- Ultra low-power architecture with three different low-power levels:
  - Sleep mode
  - Deep-sleep mode
  - Complete power-down mode
- Standard lead-free WFBGA 48-pin 4.5 x 4.5 mm package and 0.8 mm thickness

For selected STMicroelectronics sales offices' faxes:
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Full product information at www.st.com

Order code: BR2500D0108